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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,163	02/27/2002	Akira Hokazono	220110US2S	7464

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,163	HOKAZONO, AKIRA	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-19,22 and 45-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *45-62* is/are allowed.

6)☒ Claim(s) *1,2,4,6-8,11-13,15,17-19 and 22* is/are rejected.

7)☒ Claim(s) *3,5,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/05/2004 has been entered.

Drawings

2. The formal drawings filed on 02/27/2002 are acceptable.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,2,4, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over KADOSH et al. (5,818,069) in view of TSENG et al. (6,559,043).

Kadosh et al. discloses a semiconductor device having active regions connected together by an interconnect layer with first 64 and second 84 transistors formed spaced apart from each other in a semiconductor substrate 52, each of the first and second transistors having active regions 64B 84A, an isolation region 66 formed between the first 64 and second 84 transistors in the semiconductor substrate 52 for isolating the first 64 and second 84 transistors from each other, at least one slit 76, the at least one slit 76 consisting of one slit 76, formed in the surface of the isolation region 66 to allow those paired active regions 64B 84A of the first 64 and second 84 transistors which are opposed to each other with the isolation region 66 interposed therebetween to communicate with each other through it, the slit 76 having inner walls and a predetermined width, a conductive layer formed on the inner walls of the slit 76, and an interconnect layer having first and second portions (portions of part 78a which are integral thereto) respectively formed on the paired active regions 64B 84A of the first 64

and second 84 transistors so that each of them is electrically connected with a corresponding one of the paired active regions 64B 84A, and a third portion (also integral to part 78a) formed along the slit 76 on the isolation region 66, the first, second and third portions being made integral with one another, further comprising a contact portion 92 formed on the third portion of the interconnect layer, wherein the slit 76 has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit 76 can be substantially filled up with the third portion of the interconnect layer. Note figures 9-12 and column 8 lines 43-61 of Kadosh et al.

Kadosh et al. does not disclose that the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

However, Tseng et al. discloses a semiconductor device having active regions connected together by an interconnect layer having a stacked structure including a lower layer of silicon 58' and an upper layer of metal silicide 70. Note figure 10 of Tseng et al. Tseng et al. explains the advantage of patterning the lower layer 58' of silicon, then applying a blanket layer 66 of refractory metal, reacting the metal with the patterned silicon 58', and then removing the unreacted metal leaving an ohmically conductive silicide 70 in the precise pattern of patterned silicon layer 58'. Note figures 9 and 10 and column 9 lines 14-42 of Tseng et al. Therefore, it would have been obvious to a person having skill in the art to replace the interconnect layer of Kadosh et al.'s semiconductor device with the silicon/metal silicide stacked structure such as taught by

Tseng et al. in order to achieve precise patterning of the ohmically conductive silicide to thus avoid short-circuits caused by stray silicide and or metal used for the ohmic interconnect.

B. Claims 1,2,6-8,12,13, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over LIEN (5,693,975) in view of TSENG et al. (6,559,043).

With regard to claims 1,2, and 6-8, Lien discloses a semiconductor device having active regions connected together by an interconnect layer with first 641 and second 643 transistors formed spaced apart from each other in a semiconductor substrate, each of the first 641 and second 643 transistors having active regions 611a and 621a; an isolation region formed between the first 641 and second 643 transistors in the semiconductor substrate for isolating the first 641 and second 643 transistors from each other; at least one slit (the opening taken up by conductive layer 644 - see figure 6d), wherein the at least one slit consists of one slit, formed in the surface of the isolation region to allow those paired active regions 611a and 621a of the first 641 and second 643 transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width; a conductive layer 644 formed on the inner walls of the slit; and an interconnect layer 611b-621b having first and second portions respectively formed on the paired active regions 611a and 621a of the first 641 and second 643 transistors so that each of them is electrically connected with a corresponding one of the paired active regions 611a and 621a, and a third portion formed along the slit on the isolation

region, the first, second and third portions being made integral with one another, wherein a depth of the slit is less than that of the isolation region, and the conductive layer 644 is a silicon-containing film, which is polysilicon. Note figures 6a-6g of Lien.

With regard to claims12, 13, and 17-19, Lien discloses a semiconductor device having active regions connected together by an interconnect layer with first and second MOS transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second MOS transistors having a gate electrode and active regions 611a and 621a; an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other; at least one slit (the opening taken up by conductive layer 644 - see figure 6d), wherein the at least one slit consists of one slit, formed in the surface of the isolation region to allow paired active regions 611a and 621a of the first and second MOS transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width; a conductive layer 644 formed on the inner walls of the slit; a gate electrode of another MOS transistor formed above the isolation region; and an interconnect layer 611b-621b having first and second portions respectively formed on the paired active regions 611a and 621a of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions 611a and 621a, and a third portion formed along the slit on the isolation region to ride on and be electrically connected with the gate electrode of

another transistor, the first, second and third portions being made integral with one another, wherein a depth of the slit is less than that of the isolation region, and the conductive film 644 is a silicon-containing film, which is polysilicon. Note figures 6a-6g of Lien.

Lien does not disclose that the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

However, Tseng et al. discloses a semiconductor device having active regions connected together by an interconnect layer having a stacked structure including a lower layer of silicon 58' and an upper layer of metal silicide 70. Note figure 10 of Tseng et al. Tseng et al. explains the advantage of patterning the lower layer 58' of silicon, then applying a blanket layer 66 of refractory metal, reacting the metal with the patterned silicon 58', and then removing the unreacted metal leaving an ohmically conductive silicide 70 in the precise pattern of patterned silicon layer 58'. Note figures 9 and 10 and column 9 lines 14-42 of Tseng et al. Therefore, it would have been obvious to a person having skill in the art to replace the interconnect layer of Lien's semiconductor device with the silicon/metal silicide stacked structure such as taught by Tseng et al. in order to achieve precise patterning of the ohmically conductive silicide to thus avoid short-circuits caused by stray silicide and or metal used for the ohmic interconnect.

C. Claims 12,13,15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over KIM (5,573,969) in view of TSENG et al. (6,559,043).

Kim discloses a semiconductor device having active regions connected together by an interconnect layer with first and second MOS transistors formed spaced apart from each other in a semiconductor substrate 1, each of the first and second MOS transistors having a gate electrode 4 and active regions 15B 25B, an isolation region 31 formed between the first and second MOS transistors in the semiconductor substrate 1 for isolating the first and second MOS transistors from each other, at least one slit, wherein the at least one slit consists of one slit 7, formed in the surface of the isolation region 31 to allow paired active regions 15B 25B of the first and second MOS transistors which are opposed to each other with the isolation region 31 interposed therebetween to communicate with each other through it, the slit 7 having inner walls and a predetermined width, a conductive layer 35 formed on the inner walls of the slit 7, a gate electrode 4 of another MOS transistor formed above the isolation region 31, and an interconnect layer having first 15C and second 25C portions respectively formed on the paired active regions 15B 25B of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions 15B 25B, and a third portion 35 formed along the slit 7 on the isolation region 31 to ride on and be electrically connected with the gate electrode 4 of another transistor, the first 15C, second 25C, and third 35 portions being made integral with one another, and further comprising a contact portion formed on the third portion 35 of the interconnect layer, wherein the slit 7 has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit 7 can

be substantially filled up with the third portion 35 of the interconnect layer. Note figures 3C and 3E of Kim.

Kim does not disclose that the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

However, Tseng et al. discloses a semiconductor device having active regions connected together by an interconnect layer having a stacked structure including a lower layer of silicon 58' and an upper layer of metal silicide 70. Note figure 10 of Tseng et al. Tseng et al. explains the advantage of patterning the lower layer 58' of silicon, then applying a blanket layer 66 of refractory metal, reacting the metal with the patterned silicon 58', and then removing the unreacted metal leaving an ohmically conductive silicide 70 in the precise pattern of patterned silicon layer 58'. Note figures 9 and 10 and column 9 lines 14-42 of Tseng et al. Therefore, it would have been obvious to a person having skill in the art to replace the interconnect layer of Kim's semiconductor device with the silicon/metal silicide stacked structure such as taught by Tseng et al. in order to achieve precise patterning of the ohmically conductive silicide to thus avoid short-circuits caused by stray silicide and or metal used for the ohmic interconnect.

Allowable Subject Matter

6. Claims 3,5,14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 45-62 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device having active regions connected together by interconnect layers comprising: first and second transistors formed spaced apart from each other in a semiconductor substrate, each of the first, and second transistors having active regions; an isolation region formed between the first and second transistors in the semiconductor substrate for isolating the first and second transistors from each other; at least one slit formed in the surface of the isolation region to allow those paired active regions of the first and second transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width; a conductive layer formed on the inner walls of the slit; and an interconnect layer having .first and second portions respectively formed on the paired active regions of the first and second transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region, the first, second and third portions being made integral with one another, wherein the interconnect layer has a stacked

structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicide of an alloy of silicon and germanium, as recited in claim 45 or such as a semiconductor device having active regions connected together by an interconnect layer comprising: first and second MOS transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second MOS transistors having a gate electrode and active regions; an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other; at least one slit formed in the surface of the isolation region to allow paired active regions of the first and second MOS transistors, which are opposed to each other with the isolation region interposed therebetween, to communicate with each other through it, the slit having inner walls and a predetermined width; a conductive layer formed on the inner walls of the slit; a gate electrode of another MOS transistor formed above the isolation region; and an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region to ride on and be electrically connected with the gate electrode of another transistor, the first, second and third portions being made integral with one another, wherein the interconnect layer has a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicide of an alloy of silicon and germanium, as recited in claim 54.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
04/2004

Minhloan Tran
Primary Examiner
Art Unit 2826